2816
#6/a
10/5/02

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of: **NAKATA, Shunji et al.**

Group Art Unit: 2816

Serial No.: **09/871,810**

Examiner: **Cassandra F. COX**

Filed: **June 4, 2001**

P.T.O. Confirmation No.: 1974

For: **ADIABATIC CHARGING REGISTER CIRCUIT**

AMENDMENT UNDER 37 CFR §1.111

Commissioner for Patents
Washington, D.C. 20231

October 31, 2002

Sir:

In response to the Office Action dated **August 14, 2002**, please amend the above-identified application as follows:

IN THE ABSTRACT:

Delete the current Abstract and replace therewith the attached substitute Abstract.

OK to enter
CTE 01/10/03

IN THE SPECIFICATION:

Delete the current Specification and replace therewith the attached substitute Specification.

IN THE CLAIMS:

Amend claims 1, 4 and 5 as follows:

Sub B1

1. (Amended) A register circuit having a plurality of n-channel MOSFET transistors and a plurality of p-channel MOSFET transistors, accepting an input data, and a clock signal, and